REMARKS

Claims 1-20 are pending in the application. Claims 1-8, 10, 13, 14, 16, 19, and 20 stand rejected. Applicants gratefully acknowledge the Examiner's indication that claims 9, 11, 12, 15, 17 and 18 include allowable subject matter and would be allowable if rewritten as indicated. Claims 1-5, 10-11, 16, 18, 20 are amended claim 17 is cancelled without prejudice. The Examiner's reconsideration of the claim rejections is respectfully requested in view of the above amendment and the following remarks.

Claim Rejections - § 103(a)

(1) Claims 1-3, 5, 10, 16 and 19-20 are rejected as being unpatentable over Applicant's admitted prior art FIG. 1 (hereafter, "APA") in view of Nakamura (U.S. Patent Publication 2002/0154723, and in further view of Shirota (U.S. Patent Application Publication 2003/0142773), as set forth on pages 2-8 of the Office Action.

It is respectfully submitted that the combination of the APA, Nakamura, and Shirota, do not disclose or suggest, *data recovery circuit that recovers the effective data from the serial data by analyzing the sampling data to determine whether a transition has occurred in the sampling data during clock sections of the currently selected group of clock signals and selecting a different one of the groups of clock signals to be used by the oversampler based on how many of the clock sections the transition has occurred,* as recited in amended claim 1.

As shown in FIG. 1 of Applicant's disclosure, the data recovery circuit CDR does not select a different group of clock signals to be used by the oversampler 12. For example, the data recovery circuit only receives sampled data from the oversampler 12. Further the deficiencies of the APA in this regard are not cured by Nakamura. For example, Nakamura merely teaches (in para. 15) keeping a phase difference between a

set of uniform multi-phase clocks signals and another set of uniform multi-phase clock signals to a phase difference shorter than a propagation delay of a delay buffer in delay locked loops. However, Nakamura does not disclose selecting a second one of the sets for oversampling based on how many clocks sections a transition occurs in sampled data during clock sections of the first set.

The deficiencies of the APA and Nakamura with respect to the claimed data recovery circuit are not cured by Shirota. Shirota merely discloses (in para. 39-40) a circuit that selects an optimum clock signal from a group of clock signals 109 by comparing the phase position of the positive and negative edges of a receiver output signal 107 with the phase positions of each of the positive and negative edges of the clock signals in the group of clock signals 109. However, in claim 1, a new group of clock signals is essentially selected by a data recovery circuit based on data sampled using a previous group of clocks signals.

Further, in claim 1, the new group of signals is essentially chosen based on how many of the clock sections of the previous group a transition has occurred in the sampled data. For example, if a transition has occurred in all of the clock sections, the current group of clocks signals used by the oversampler may be deselected, and a new and different group of clock signals may be selected. (See p.21, 3-8 and p.23, 7-17 of Applicant's disclosure). However, in Shirota, a new clock signal is chosen based on the phase position of its positive and negative edges and the phase position of the positive and negative edges of the receiver output signal 107. The new clock signal is not chosen based on how many clock sections data sampled from the receiver output signal 107

experiences a transition. Further, only a single new clock signal is chosen and not a group of clock signals.

In addition, Shirota merely discloses (in para. 11) synchronizing the receiver output signal 107 with a recovered clock signal and not use of a clock signal to oversample serial data, and especially not use of at least two clocks signals to oversample serial data.

For at least the foregoing reasons, claim 1 is believed to be patentable over the combination of the APA, Nakamura, and Shirota.

Claim 20 is believe to be patentable over said combination for reasons similar to claim 1. For example, claim 20 has been amended, *inter alia*, to recite, *analyzing the latched OSR bits to determine whether a transition has occurred in the sampling data during clock sections of the selected set of OSR sampling clock signals* and *selecting the other set of OSR sampling clocks signals for subsequent oversampling of each bit of the serial data based on how many of the clocks sections the transition has occurred.*

Claim 16 has been amended to incorporate the subject matter from allowable claim 17. Thus, claim 16 is patentable over the combination of APA, Nakamura, and Shirota.

Allowable claim 11 has been re-written in independent form to include subject matter dependent claims 1 and 2. Thus, claim 11 is patentable over the combination of APA, Nakamura, and Shirota.

Claims 2-3, 5, 10 are believed to be patentable over said combination at least by virtue of their dependence from claim 1, and claim 19 is believed to be patentable over said combination at least by virtue of its dependence from claim 16.

(2) Claims 4 and 6 are rejected as being unpatentable over <u>APA</u>, <u>Nakamura</u>, <u>Shirota</u>, and U.S. Patent 6,807,233 to <u>Sato</u>, **(3)** Claim 7 is rejected as being unpatentable over <u>APA</u>, <u>Nakamura</u>, <u>Shirota</u> and U.S. Patent 5,528,198 to <u>Baba</u>, and **(4)** Claim 8 is rejected as being unpatentable over <u>APA</u>, <u>Nakamura</u>, <u>Shirota</u> and U.S. Patent 7,103,343 to <u>Boss</u>.

The above obviousness rejections (2~4) are legally deficient as a matter of law at least to the extent that the rejections are premised on the combination of <u>APA</u>, <u>Nakamura</u>, and <u>Shirota</u>, at least for the reasons stated above for the base claim 1, from which claims 4, 6, 7, and 8 depend.

Withdrawal of the claim rejections under 35 U.S.C. § 103 is respectfully requested.

Conclusion

In view of the foregoing remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration is respectfully requested.

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